Amendments to the Specification:

Please replace paragraphs [0001], [0032], [0036], and [0057] with the following amended paragraphs:

[0001] The present disclosure is related to the following commonly-assigned co-pending U.S. Patent Applications: ~~No. _____~~ No. 10/643,072 ~~(Attorney Docket No. 019680-006000US)~~, filed on the same date as the present application, entitled "Private Addressing in a Multi-Processor Graphics Processing System", now U.S. Patent No. 6,956,579, issued October 18, 2005; and ~~No. _____~~ No. 10/639,893, ~~(Attorney Docket No. 019680-005900US), filed _____~~ filed August 12, 2003, entitled "Programming Multiple Chips from a Command Buffer," the respective disclosures of which are incorporated herein by reference for all purposes.

[0032] Bridge unit 130 is configured to manage communication between components of graphics processing subsystem 112 (including memory interfaces 123a, 123b) and other components of system 100. For example, bridge unit 130 may receive all incoming data transfer requests from system bus 106 and distribute (or broadcast) the requests to one or more of memory interfaces 123a, 123b. Bridge unit 130 may also receive data transfer requests originating from components of graphics processing subsystem 112 (such as GPUs 114a, 114b) that reference memory locations external to graphics processing subsystem 112 and transmit these requests via system bus 106. In addition, in some embodiments, bridge unit 130 facilitates access by either of GPUs 114a, 114b to the memory 116b, 116a associated with the other of GPUs 114a, 114b. Examples of implementations of bridge unit 130 are described in detail in the above-referenced co-pending application No. 10/643,072; ~~(Attorney Docket No. 019680-006000US);~~ a detailed description is omitted herein as not being critical to understanding the present invention.

[0036] The command buffer may be of fixed size (e.g., 5 megabytes) and may be written and read in a wraparound fashion (e.g., after writing to the last location, CPU 102 may reset the "put" pointer to the first location). A more detailed description of embodiments of command buffers and techniques for writing commands and data to command buffers in a multi-chip graphics processing system is provided in the above-referenced co-pending application No. 10/639,893. ~~(Attorney Docket No. 019680-005900US).~~

[0057] In some embodiments, when the boundary line is shifted to balance the load, it may be useful to transfer data from one display buffer to another. For example, in Fig. 2, suppose that just after GPUs 114a, 114b have finished rendering a current frame, the value of P is changed to a larger value P', increasing the number of lines that GPU 114a will render for the next frame. GPU 114a may need access to data for some or all of lines P+1 through P' of the current frame in order to correctly process the next frame. In one embodiment, GPU 114a can obtain the data by a DMA transfer from the portion of display buffer 122b that has the data for lines P+1 through P'. Examples of processes that can advantageously be used for this purpose are described in the above-referenced application No. 10/643,072, ~~(Attorney Docket No. 019680-006000US),~~ although numerous other processes for transferring data may also be used. It is to be understood that transferring data between display buffers is not required but may be useful in embodiments where any overhead associated with the data transfer is outweighed by the overhead of having one GPU repeat computations previously performed by another GPU. Transferring data that is not displayed (e.g., texture data) between graphics memories 116a, 116b may also be desirable in some instances and can be implemented using any of the techniques mentioned above.